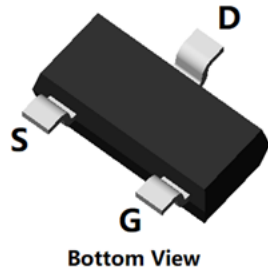
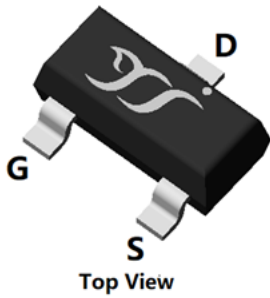
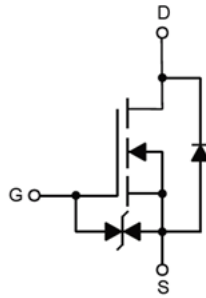


## N-Channel Enhancement Mode Field Effect Transistor



**SOT-23**



### Product Summary

- $V_{DS}$  50V
- $I_D$  0.22A
- $R_{DS(ON)}$  ( at  $V_{GS}=10V$  )  $< 1.6\Omega$
- $R_{DS(ON)}$  ( at  $V_{GS}=4.5V$  )  $< 2.5\Omega$
- $R_{DS(ON)}$  ( at  $V_{GS}=2.5V$  )  $< 3.8\Omega$
- Gate-Source ESD Rating Up to 1.5KV (HBM)

### General Description

- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

### Applications

- Power Management Functions
- Load switch
- DC-DC convertor

### ■ Absolute Maximum Ratings ( $T_J=25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			$V_{DS}$	50	V
Gate-source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current (Note 1,2)	Steady-State	$T_A=25^\circ\text{C}$	$I_D$	0.22	A
		$T_A=100^\circ\text{C}$		0.14	
Pulsed Drain Current	$T_C=25^\circ\text{C}, t_p=100\mu\text{s}$		$I_{DM}$	1	A
Total Power Dissipation (Note 1,2)	Steady-State	$T_A=25^\circ\text{C}$	$P_D$	0.61	W
		$T_A=100^\circ\text{C}$		0.24	
Junction and Storage Temperature Range			$T_J, T_{STG}$	-55~+150	$^\circ\text{C}$

### ■ Thermal resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	202	$^\circ\text{C/W}$

### ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
BSS138AJKQ	F2	.SS	3000	30000	120000	7" reel



# BSS138AJKQ

## ■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	50	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	-	-	100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V	-	-	±5	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	0.7	1	1.45	V
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.5A	-	1.2	1.6	Ω
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.1A	-	1.24	2.5	
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =0.1A	-	1.8	3.8	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =0.22A, V <sub>GS</sub> =0V	-	-	1.2	V
Gate resistance	R <sub>G</sub>	f=1MHz	-	75	-	Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>		-	-	0.22	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz	-	29	-	pF
Output Capacitance	C <sub>oss</sub>		-	4.3	-	
Reverse Transfer Capacitance	C <sub>riss</sub>		-	3	-	
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =25V, I <sub>D</sub> =0.5A	-	1.2	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	0.15	-	
Gate-Drain Charge	Q <sub>gd</sub>		-	0.31	-	
Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> =0.5A, di/dt=100A/us	-	2.1	-	nC
Reverse Recovery Time	t <sub>rr</sub>		-	9.2	-	ns
Turn-on Delay Time	t <sub>D(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =25V, I <sub>D</sub> =0.5A R <sub>GEN</sub> =25Ω	-	3	-	ns
Turn-on Rise Time	t <sub>r</sub>		-	2.7	-	
Turn-off Delay Time	t <sub>D(off)</sub>		-	11	-	
Turn-off fall Time	t <sub>f</sub>		-	8.1	-	

Note:

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- The value of R<sub>θJA</sub> is measured with the device mounted on the 40mm\*40mm\*1.1mm single layer FR-4 PCB board with 1 in<sup>2</sup> pad of 2oz. Copper, in the still air environment with TA =25°C. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.



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## Typical Electrical and Thermal Characteristics Diagrams

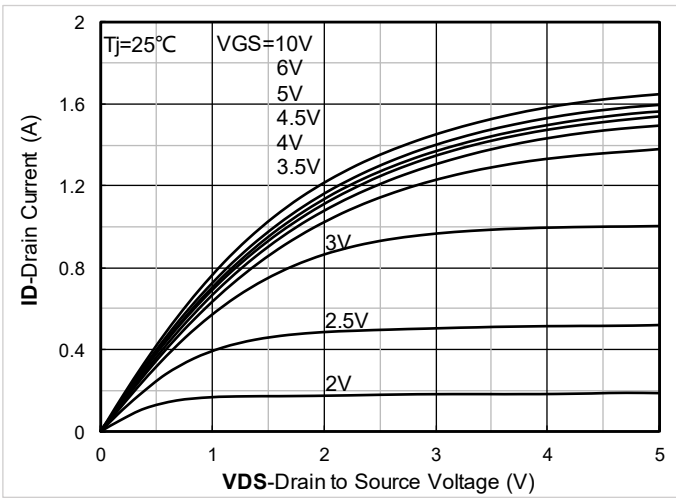


Figure 1. Output Characteristics

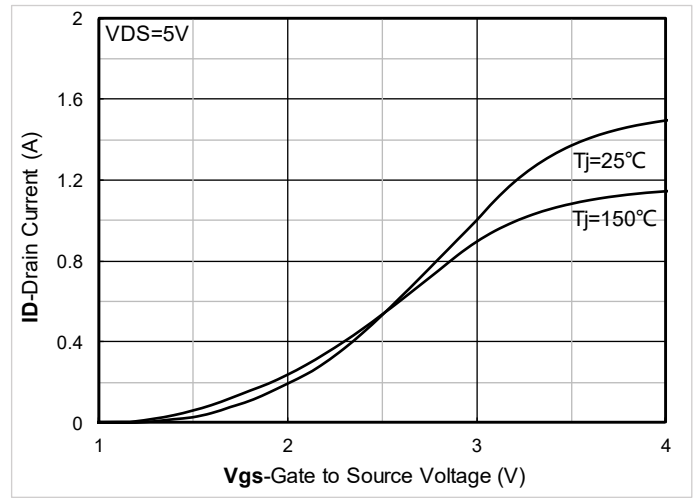


Figure 2. Transfer Characteristics

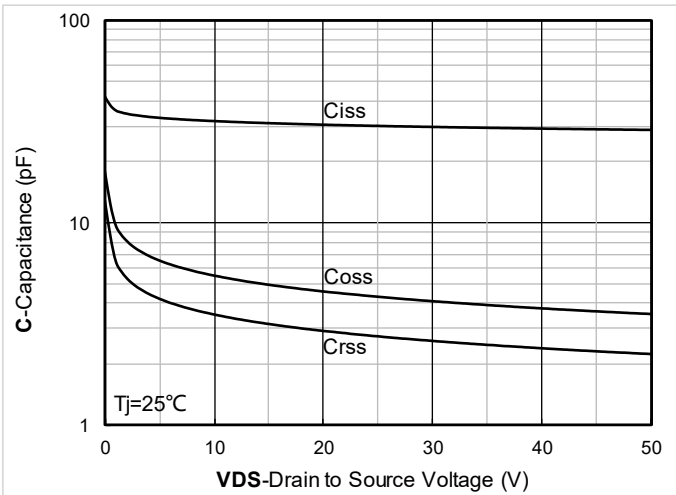


Figure 3. Capacitance Characteristics

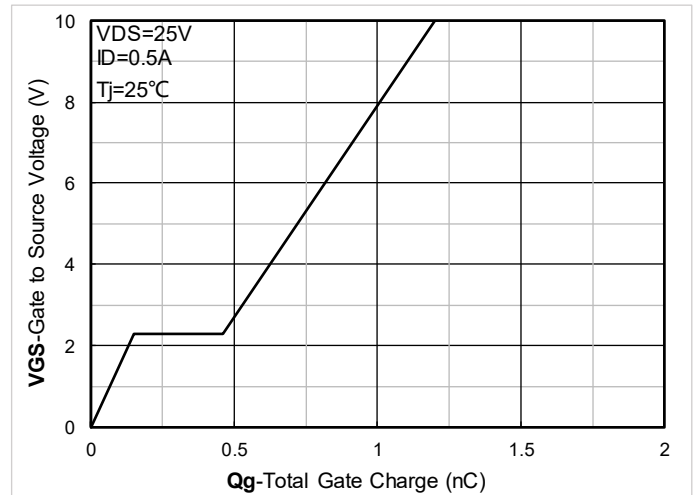


Figure 4. Gate Charge

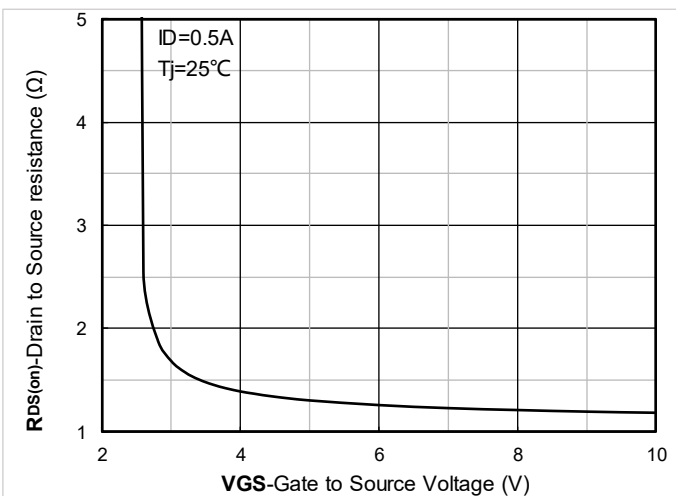


Figure 5. On-Resistance vs Gate to Source Voltage

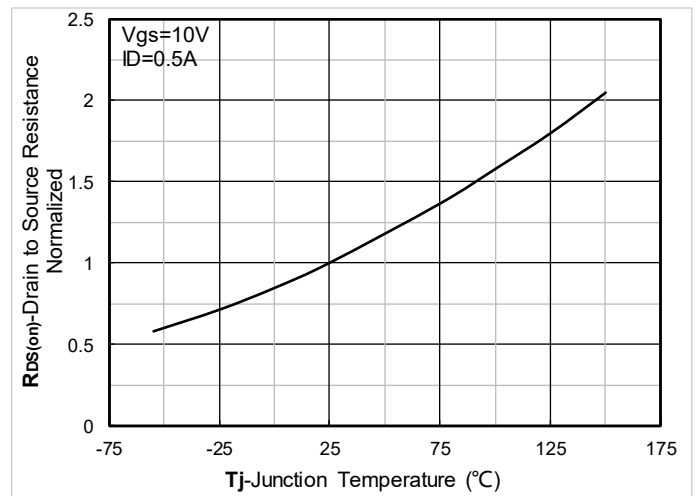


Figure 6. Normalized On-Resistance



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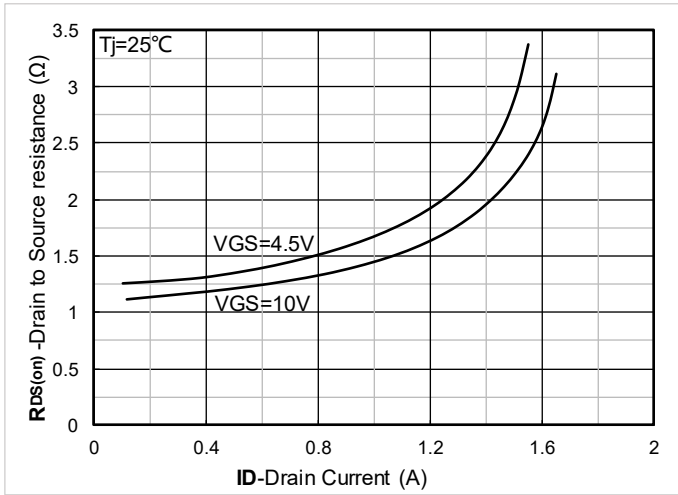


Figure 7.  $R_{DS(on)}$  VS Drain Current

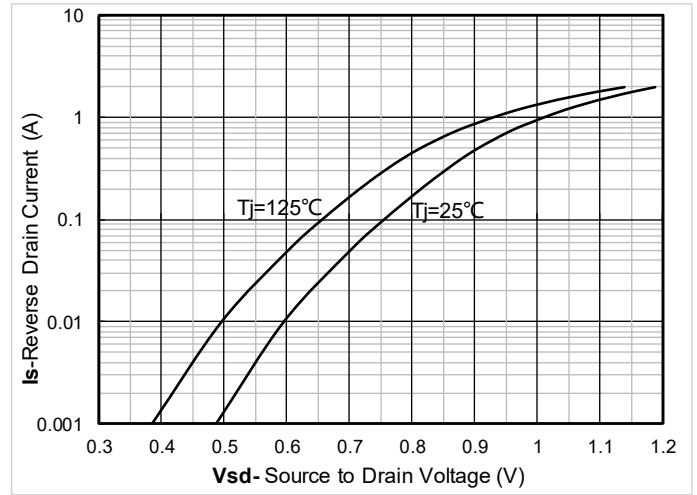


Figure 8. Forward characteristics of reverse diode

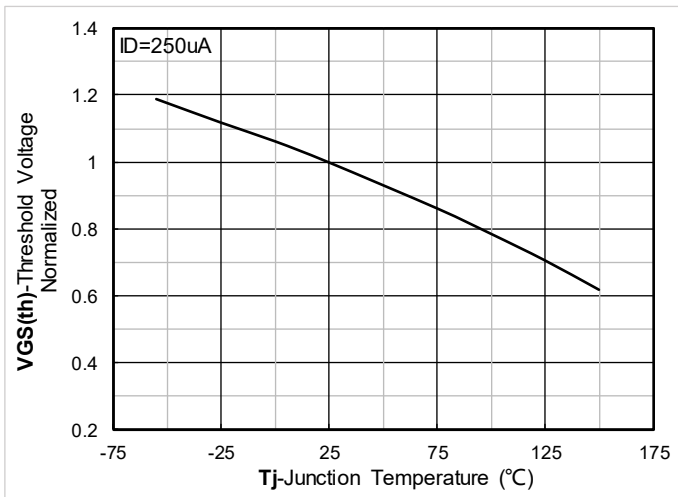


Figure 9. Normalized Threshold voltage

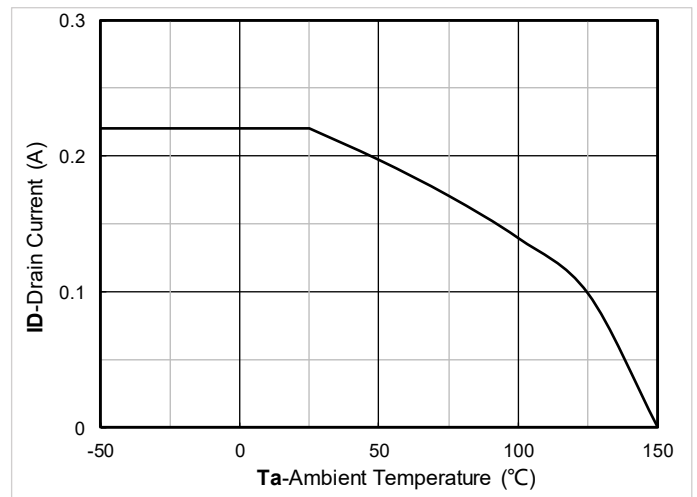


Figure 10. Current dissipation

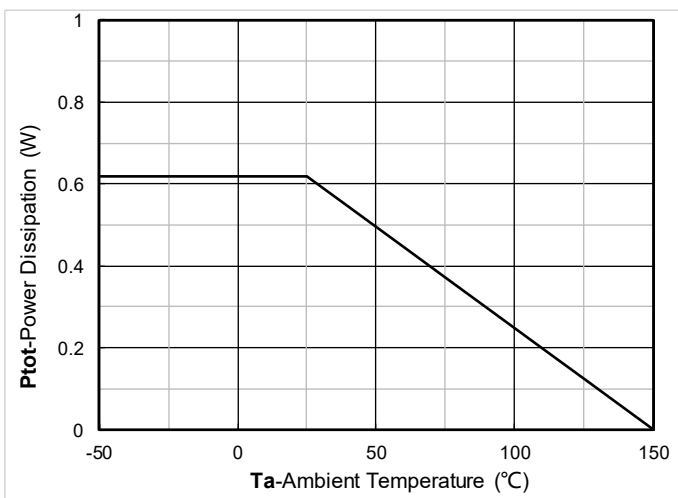


Figure 11. Power dissipation

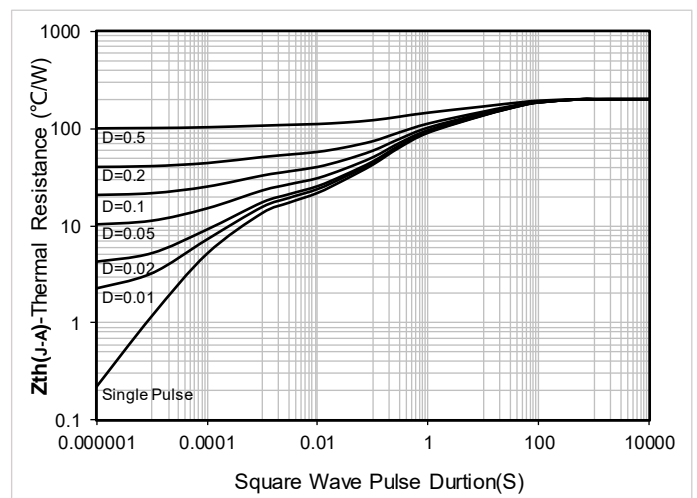
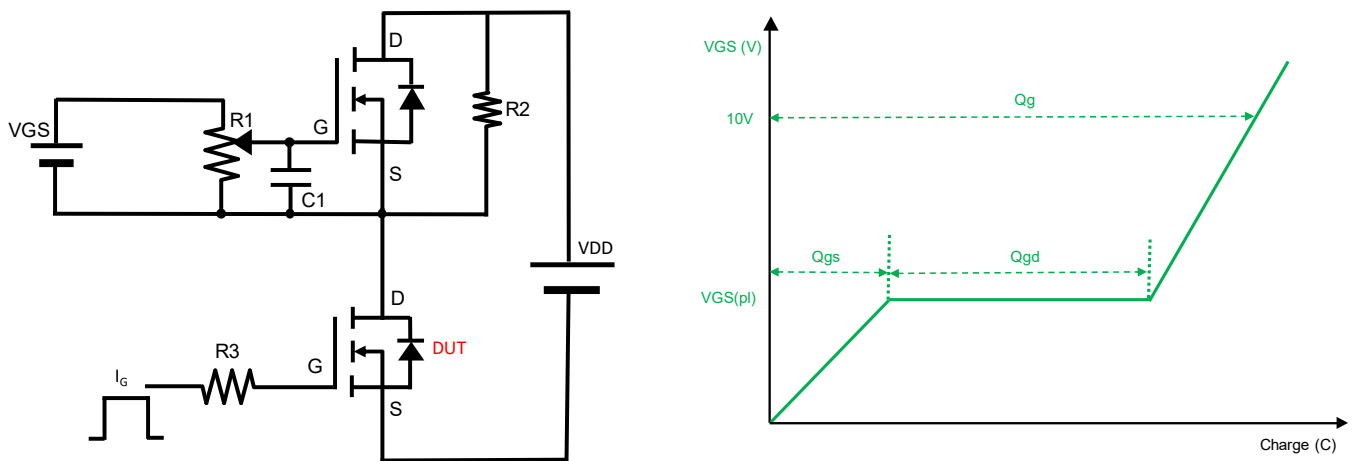
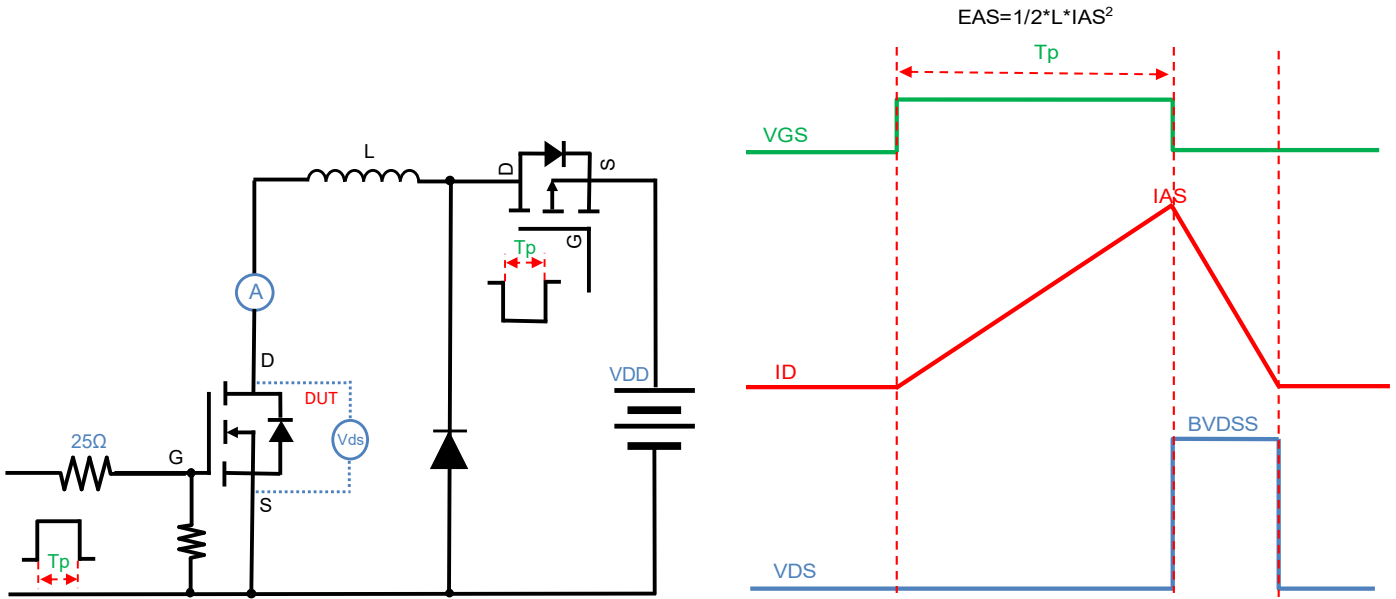


Figure 12. Maximum Transient Thermal Impedance

## ■ Test Circuits & Waveforms



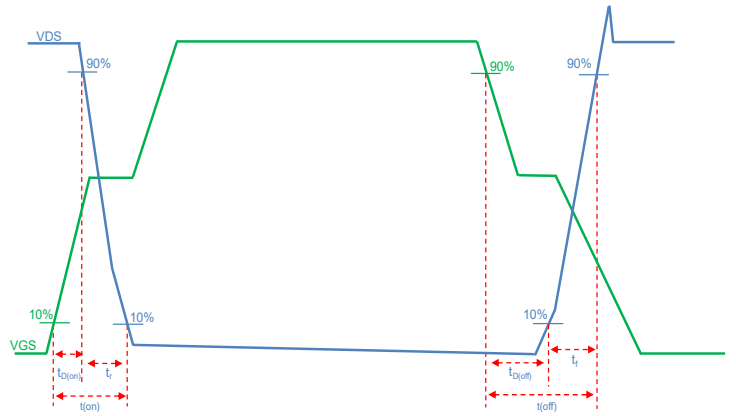
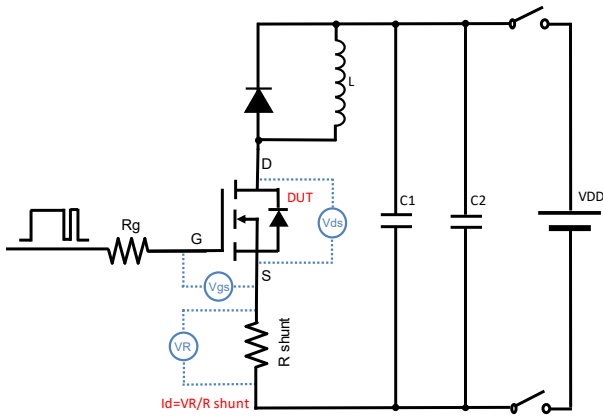


Figure C. Resistive Switching Test Circuit & Waveform

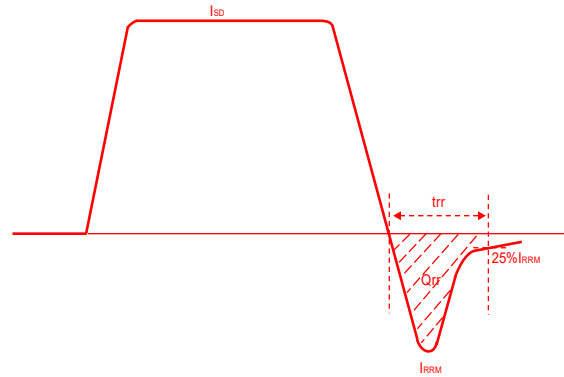
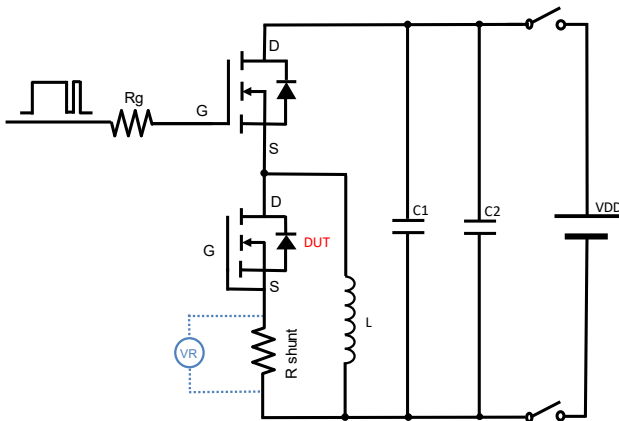
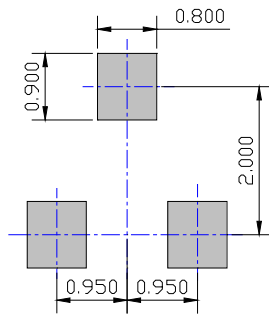
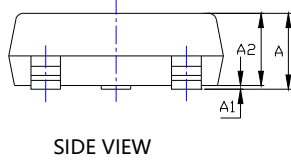
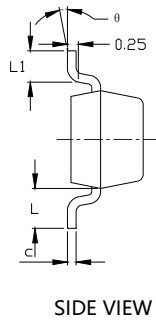
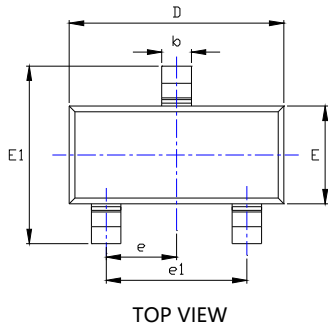


Figure D. Diode Recovery Test Circuit & Waveform



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## ■ SOT-23 Package information



UNIT: mm

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037 TYP		0.950 TYP	
e1	0.071	0.079	1.800	2.000
L	0.022 REF		0.550 REF	
L1	0.012	0.020	0.300	0.500
θ	0°	8°	0°	8°

NOTE:  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



## BSS138AJKQ

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